Application Serial No. 10/712,921 Reply to Office Action of February 8, 2005

PATENT

Docket: CU-3455

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re Application:

Chang Yeol Lee et al.

GRP ART UNIT: 2813

MAR 0 8 2005

Serial No:

10/712,921

Ex.: Chen, Jack S.J.

Filed: November 13, 2003

For:

Method For Reducing Poly-Depletion In Dual Gate

CMOS Fabrication Process

Certification under 37 C.F.R. §1.8(a)

The USPTO Central Fax No. (703) 872-9306

Date of Fax Transmittal: March 3, 2005

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted to the United States Patent and Trademark Office to the

fax number and on the date indicated above.

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The Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

RESPONSE TO RESTRICTION REQUIREMENT

In the Office Action dated February 8, 2005, setting a 1-month shortened statutory period for a reply ending on March 8, 2005, the pending Claims 1-10 were restricted as follows:

Species I: Claims 1-4 drawn to a method of forming a semiconductor device

according to a first embodiment;

Species II: Claim 5 drawn to a method of forming a semiconductor device

according to a second embodiment;

Species III: Claims 6-7 drawn to a method of forming a semiconductor device

according to a third embodiment; and

Species IV: Claims 8-10 drawn to a method of forming a semiconductor device

according to a fourth embodiment.

Applicant hereby elects Species I: Claims 1-4.

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In view of the Examiner's earlier restriction requirement, Applicants retain the right to present the non-elected in a divisional application.

Respectfully submitted,

Dated: March 2, 2005

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